IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

1.   (Original)   A read channel, comprising:

an equalizer configured to equalize a digital signal to provide equalized reproduced signals; and

a Viterbi detector capable of receiving the equalized reproduced signals and converting the reproduced signals into a digital output signal indicative of data stored on a recording medium;

wherein the equalizer is implemented using a coefficient learning circuit that adaptively updates coefficients for the equalizer based upon a cosine function.

2.   (Original)   The read channel of claim 1, wherein the coefficient learning circuit adjusts coefficients using a tap coefficient update equation having a first parameter, k, for modifying a magnitude response.

3.   (Previously Presented)   The read channel of claim 2, wherein the first parameter, k, is adjusted according to $k = k - g*(f(a_{k+1}) + f(a_{k-1}))*e_k$, where k is the cosine equalizer parameter for modifying the magnitude response, g is an update attenuation gain, $f(\ )$ is a predetermined cosine function, a_{k+1} represents a bit to be detected at time k+1, a_{k-1} represents a bit to be detected at time k-1, and e_k is an error signal based on a difference between a noisy equalized signal and a desired noiseless signal.

1   4.   (Original)   The read channel of claim 2, wherein the coefficient

2 learning circuit adjusts coefficients using a tap coefficient update equation having a

3 second parameter, j, for modifying a phase response.

1   5.   (Previously Presented)   The read channel of claim 4, wherein the

2 second parameter, j, is adjusted according to $j = j - g*(f(a_{k+2}) + f(a_{k-2}))*e_k$, where j is the

3 cosine equalizer parameter for modifying the phase response, g is an update attenuation

4 gain, f( ) is a predetermined cosine function, a_{k+2} represents a bit to be detected at time

5 k+2, a_{k-2} represents a bit to be detected at time k-2, and e_k is an error signal based on a

6 difference between a noisy equalized signal and a desired noiseless signal.

1   6.   (Original)   The read channel of claim 1, wherein the coefficient

2 learning circuit adjusts coefficients using a tap coefficient update equation having a

3 parameter, j, for modifying a phase response.

1   7.   (Currently Amended) The read channel of claim 1, wherein the coefficient

2 learning circuit adjusts coefficients, w_i, according to $w_i = w_i - g*f(a_{k-i})*e_k$, where g is a

3 provided update attenuation gain and [[$f(a_{k-i})$]] <u>f( )</u> is a predetermined cosine function

4 and [[a_{k+i}]] <u>a_{k-i}</u> represents a bit to be detected at time [[k+I]] <u>k-i</u>.

1   8.   (Original)   The read channel of claim 7, wherein $f(a_{k-i})$ is chosen to be

2 $a_{k-i} - a_{k-i-2}$, wherein written bits that are to be detected, a_{k-i}, are convolved with a PR4

3 response based upon the cosine function.

1   9.   (Original)   The read channel of claim 7, wherein $f(a_{k-i})$ is chosen to be

2    $a_{k-i} + a_{k-i-1} - a_{k-i-2} - a_{k-i-3}$, wherein written bits that are to be detected, a_{k-i}, are convolved

3   with the EPR4 response based upon the cosine function.

1   10.   (Original)   The read channel of claim 7, wherein $f(a_{k-i})$ is chosen to be

2    $a_{k-i}t_k$, wherein written bits that are to be detected, a_{k-i}, are convolved with t_k based upon

3   the cosine function.

1   11.   (Original)   The read channel of claim 7, wherein $f(a_{k-i})$ is chosen to be

2    $a_{k-i}h_k$, wherein written bits that are to be detected, a_{k-i}, are convolved with h_k based upon

3   the cosine function.

1   12.   (Original)   A waveform equalizer that equalizes a waveform of a

2   reproduction signal obtained by reproducing marks and non-marks recorded on a

3   recording medium, comprising:

4   a delay element that delays a propagation of the reproduced signal;

5   a plurality of multipliers that multiply predetermined coefficients by the

6   reproduction signal and the delayed signal from the delay element;

7   a coefficient learning circuit that adaptively updates the predetermined

8   coefficients for each of the plurality of multipliers; and

9   an adder that adds outputs from the plurality of multipliers;

10   wherein the coefficient learning circuit adaptively updates coefficients for the

11   equalizer based upon a cosine function.

1   13.   (Original)   The waveform equalizer of claim 12, wherein the

2   coefficient learning circuit adjusts coefficients using a tap coefficient update equation

3   having a first parameter, k, for modifying a magnitude response.

1   14.   (Previously Presented)   The waveform equalizer of claim 13,

2   wherein the first parameter, k, is adjusted according to $k=k-g*(f(a_{k+1})+f(a_{k-1}))*e_k$, where k

3   is the cosine equalizer parameter for modifying the magnitude response, g is an update

4   attenuation gain, f( ) is a predetermined cosine function, a_{k+1} represents a bit to be

5   detected at time k+1, a_{k-1} represents a bit to be detected at time k-1, and e_k is an error

6   signal based on a difference between a noisy equalized signal and a desired noiseless

7   signal.

1   15.   (Original)   The waveform equalizer of claim 13, wherein the

2   coefficient learning circuit adjusts coefficients using a tap coefficient update equation

3   having a second parameter, j, for modifying a phase response.

1   16.   (Previously Presented)   The waveform equalizer of claim 15,

2   wherein the second parameter, j, is adjusted according to $j=j-g*(f(a_{k+2})+f(a_{k-2}))*e_k$, where

3   j is the cosine equalizer parameter for modifying the phase response, g is an update

4   attenuation gain, f( ) is a predetermined cosine function, a_{k+2} represents a bit to be

5   detected at time k+2, a_{k-2} represents a bit to be detected at time k-2, and e_k is an error

6   signal based on a difference between a noisy equalized signal and a desired noiseless

7   signal.

1   17.   (Original)   The waveform equalizer of claim 12, wherein the

2   coefficient learning circuit adjusts coefficients using a tap coefficient update equation

3   having a parameter, j, for modifying a phase response.

1   18.   (Currently Amended) The waveform equalizer of claim 12, wherein the

2   coefficient learning circuit adjusts coefficients, w_i, according to $w_i = w_i - g*f(a_{k-i})*e_k$,

3   where g is a provided update attenuation gain and and [[$f(a_{k-i})$]] f( ) is a predetermined

4   cosine function and [[a_{k+i}]] a_{k-i} represents a bit to be detected at time [[k+I]] k-i.

1   19.   (Original)   The waveform equalizer of claim 18, wherein $f(a_{k-i})$ is

2   chosen to be $a_{k-i} - a_{k-i-2}$, wherein written bits that are to be detected, a_{k-i} , are convolved

3   with a PR4 response based upon the cosine function.

1   20.   (Original)   The waveform equalizer of claim 18, wherein $f(a_{k-i})$ is

2   chosen to be $a_{k-i} + a_{k-i-1} - a_{k-i-2} - a_{k-i-3}$, wherein written bits that are to be detected, a_{k-i} , are

3   convolved with the EPR4 response based upon the cosine function.

1   21.   (Original)   The waveform equalizer of claim 18, wherein $f(a_{k-i})$ is

2   chosen to be $a_{k-i}t_k$, wherein written bits that are to be detected, a_{k-i} , are convolved with t_k

3   based upon the cosine function.

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1   22.   (Original)   The waveform equalizer of claim 18, wherein $f(a_{k-i})$ is

2   chosen to be $a_{k-i}h_k$, wherein written bits that are to be detected, a_{k-i}, are convolved with h_k

3   based upon the cosine function.

1   23.   (Original)   A signal processing system, comprising:

2   memory for storing data therein; and

3   a processor, coupled to the memory, for equalizing a digital signal to provide

4   equalized reproduced signals, the processor adaptively updates coefficients for the

5   equalizer based upon a cosine function.

1   24.   (Original)   The signal processing system of claim 23, wherein the

2   processor adjusts coefficients using a tap coefficient update equation having a first

3   parameter, k, for modifying a magnitude response.

1   25.   (Previously Presented)   The signal processing system of claim 24,

2   wherein the first parameter, k, is adjusted according to $k=k-g*(f(a_{k+1})+f(a_{k-1}))*e_k$, where k

3   is the cosine equalizer parameter for modifying the magnitude response, g is an update

4   attenuation gain, f( ) is a predetermined cosine function, a_{k+1} represents a bit to be

5   detected at time k+1, a_{k-1} represents a bit to be detected at time k-1, and e_k is an error

6   signal based on a difference between a noisy equalized signal and a desired noiseless

7   signal.

1   26.   (Original)   The signal processing system of claim 24, wherein the

2   processor adjusts coefficients using a tap coefficient update equation having a second

3   parameter, j, for modifying a phase response.

1   27.   (Previously Presented)   The signal processing system of claim 26,

2   wherein the second parameter, j, is adjusted according to $j=j-g*(f(a_{k+2})+f(a_{k-2}))*e_k$, where

3   j is the cosine equalizer parameter for modifying the phase response, g is an update

4   attenuation gain, f( ) is a predetermined cosine function, a_{k+2} represents a bit to be

5   detected at time k+2, a_{k-2} represents a bit to be detected at time k-2, and e_k is an error

6   signal based on a difference between a noisy equalized signal and a desired noiseless

7   signal.

1   28.   (Original)   The signal processing system of claim 23, wherein the

2   processor adjusts coefficients using a tap coefficient update equation having a parameter,

3   j, for modifying a phase response.

1   29.   (Currently Amended) The signal processing system of claim 23, wherein

2   the coefficient learning circuit adjusts coefficients, w_i, according to $w_i=w_i-g*f(a_{k-i})*e_k$,

3   where g is a provided update attenuation gain and and [[$f(a_{k-i})$]] <u>f( )</u> is a predetermined

4   cosine function and [[a_{k+i}]] <u>a_{k-i}</u> represents a bit to be detected at time [[k+I]] <u>k-i</u>.

1   30.   (Original)   The signal processing system of claim 29, wherein $f(a_{k-i})$ is

2   chosen to be $a_{k-i} - a_{k-i-2}$, wherein written bits that are to be detected, a_{k-i}, are convolved

3   with a PR4 response based upon the cosine function.

1   31.   (Original)   The signal processing system of claim 29, wherein $f(a_{k-i})$ is

2   chosen to be $a_{k-i} + a_{k-i-1} - a_{k-i-2} - a_{k-i-3}$, wherein written bits that are to be detected, a_{k-i}, are

3   convolved with the EPR4 response based upon the cosine function.

1   32.   (Original)   The signal processing system of claim 29, wherein $f(a_{k-i})$ is

2   chosen to be $a_{k-i} t_k$, wherein written bits that are to be detected, a_{k-i}, are convolved with t_k

3   based upon the cosine function.

1   33.   (Original)   The signal processing system of claim 29, wherein $f(a_{k-i})$ is

2   chosen to be $a_{k-i} h_k$, wherein written bits that are to be detected, a_{k-i}, are convolved with h_k

3   based upon the cosine function.

1   34.   (Original)   A magnetic storage device, comprising:

2   a magnetic storage medium for recording data thereon;

3   a motor for moving the magnetic storage medium;

4   a head for reading and writing data on the magnetic storage medium;

5   an actuator for positioning the head relative to the magnetic storage medium; and

6   a data channel for processing encoded signals on the magnetic storage medium,

7   the data channel comprising an equalizer configured to equalize a digital signal to

8   provide equalized reproduced signals and a Viterbi detector capable of receiving the

9   equalized reproduced signals and converting the reproduced signals into a digital output

10   signal indicative of data stored on a recording medium; wherein the equalizer is

11   implemented using a coefficient learning circuit that adaptively updates coefficients for

12   the equalizer based upon a cosine function.

1   35.   (Original)   The magnetic storage device of claim 34, wherein the

2   equalizer adjusts coefficients using a tap coefficient update equation having a first

3   parameter, k, for modifying a magnitude response.

1   36.   (Previously Presented)   The magnetic storage device of claim 35,

2   wherein the first parameter, k, is adjusted according to $k=k-g*(f(a_{k+1})+f(a_{k-1}))*e_k$, where k

3   is the cosine equalizer parameter for modifying the magnitude response, g is an update

4   attenuation gain, f( ) is a predetermined cosine function, a_{k+1} represents a bit to be

5   detected at time k+1, a_{k-1} represents a bit to be detected at time k-1, and e_k is an error

6   signal based on a difference between a noisy equalized signal and a desired noiseless

7   signal.

1   37.   (Original)   The magnetic storage device of claim 35, wherein the

2   equalizer adjusts coefficients using a tap coefficient update equation having a second

3   parameter, j, for modifying a phase response.

1   38.   (Previously Presented)   The magnetic storage device of claim 37,

2   wherein the second parameter, j, is adjusted according to $j=j-g*(f(a_{k+2})+f(a_{k-2}))*e_k$, where

3   j is the cosine equalizer parameter for modifying the phase response, g is an update

4   attenuation gain, f( ) is a predetermined cosine function, a_{k+2} represents a bit to be

5   detected at time k+2, a_{k-2} represents a bit to be detected at time k-2, and e_k is an error

6   signal based on a difference between a noisy equalized signal and a desired noiseless

7   signal.

1   39.   (Original)   The magnetic storage device of claim 34, wherein the

2   equalizer adjusts coefficients using a tap coefficient update equation having a parameter,

3   j, for modifying a phase response.

1   40.   (Currently Amended) The magnetic storage device of claim 34, wherein

2   the coefficient learning circuit adjusts coefficients, w_i, according to $w_i = w_i - g * f(a_{k-i}) * e_k$,

3   where g is a provided update attenuation gain and and [[$f(a_{k-i})$]] $\underline{f(\ )}$ is a predetermined

4   cosine function and [[a_{k+i}]] $\underline{a_{k-i}}$ represents a bit to be detected at time [[k+I]] $\underline{k-i}$.

1   41.   (Original)   The magnetic storage device of claim 40, wherein $f(a_{k-i})$ is

2   chosen to be $a_{k-i} - a_{k-i-2}$, wherein written bits that are to be detected, a_{k-i}, are convolved

3   with a PR4 response based upon the cosine function.

1   42.   (Original)   The magnetic storage device of claim 40, wherein $f(a_{k-i})$ is

2   chosen to be $a_{k-i} + a_{k-i-1} - a_{k-i-2} - a_{k-i-3}$, wherein written bits that are to be detected, a_{k-i}, are

3   convolved with the EPR4 response based upon the cosine function.

1   43.   (Original)   The magnetic storage device of claim 40, wherein $f(a_{k-i})$ is

2   chosen to be $a_{k-i} t_k$, wherein written bits that are to be detected, a_{k-i}, are convolved with t_k

3   based upon the cosine function.

1   44.   (Original)   The magnetic storage device of claim 40, wherein $f(a_{k-i})$ is

2   chosen to be $a_{k-i} h_k$, wherein written bits that are to be detected, a_{k-i}, are convolved with h_k

3   based upon the cosine function.

1   45.   (Original)   A read channel, comprising:

2   means for equalizing a digital signal to provide equalized reproduced signals; and

3   means, coupled to the means for equalizing, for receiving the equalized

4 reproduced signals and converting the reproduced signals into a digital output signal

5 indicative of data stored on a recording medium;

6   wherein the means for equalizing is implemented using means for adaptively

7 updating coefficients for the means for equalizing based upon a cosine function.

1   46.   (Original)   A waveform equalizer that equalizes a waveform of a

2 reproduction signal obtained by reproducing marks and non-marks recorded on a

3 recording medium, comprising:

4   means for delaying propagation of a reproduced signal;

5   means for multiplying predetermined coefficients by the reproduced signal and

6 the delayed signal from the means for delaying;

7   means for adaptively updating the predetermined coefficients for the means for

8 multiplying; and

9   means for adding outputs from the means for multiplying;

10   wherein the means for adaptively updating the predetermined coefficients updates

11 the predetermined coefficients based upon a cosine function.